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Hexagonal Boron Nitride for Nanoscale Heat Dissipation in Electronic and Photonic Chips

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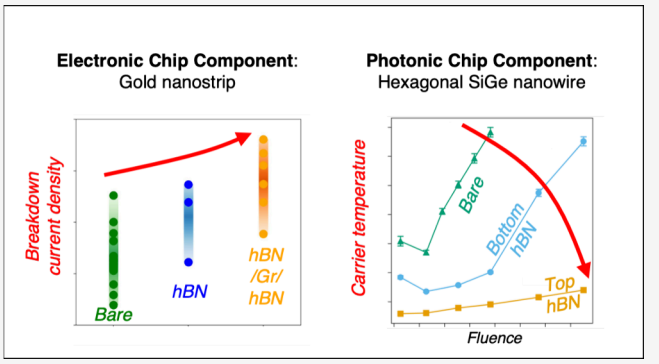
ABSTRACT: Efficient heat dissipation is critical for chip components, in particular around (sub)microscopic regions with locally elevated power densities, where performance degradation and failure can originate. Here, we experimentally demonstrate enhanced heat dissipation using hexagonal boron nitride (hBN) flakes and heterostructures on gold nanostrips and hexagonal SiGe nanowires. These nanoscale building blocks for electronic and photonic chips simultaneously serve as local temperature sensors. We transferred flakes using dry transfer, ensuring pristine interfaces. Covering gold nanostrips with hBN flakes or hBN/graphene/hBN stacks decreases the temperature ramp rate by up to 40%, and increases the breakdown current density by up to 30%. This occurs through improved in-plane heat dissipation, according to our simulations. Covering hexagonal SiGe nanowires with hBN decreases the operating temperature by up to 500 K under optical excitation, due to improved thermal boundary conductance. These findings pave the way for targeted thermal management in miniaturized electronic and photonic devices.



KEYWORDS: *2D materials, thermal management, hotspots, hBN, graphene, nanowires*

Smart devices have become deeply embedded in our daily lives, driving an ever-growing demand for electronic and photonic chips with higher computational power and greater integration density.[1,2] However, the reduced thermal conductivities of nanoscale components[3,4] provide a critical challenge to efficiently dissipate heat when chips are further miniaturized. The reduced thermal conductivities at the nanoscale also limit the ability to operate at high power densities.[5,6] Since thermal failure[7,8] often originates from (sub)micrometer-sized "hotspot" regions of electronic and photonic chips, anisotropic heat spreaders that enable efficient heat dissipation in a preferred direction are promising in reducing thermal breakdown.

Two-dimensional (2D) materials are attractive heat-spreading candidates due to their mechanical flexibility and strong thermal anisotropy.[9−16] Among them, hexagonal boron nitride (hBN) stands out for its high in-plane thermal conductivity of 400 W m^{-1} K^{-1},[1,14] excellent electrical insulation—in contrast to graphene—and broadband optical transparency.[17] Previous studies have shown that hBN films can enhance heat dissipation through the global cooling of large-area electronic and photonic devices.[16,18−20] However, since thermal breakdown often starts at localized hotspots, the most efficient approach to limit device failure is to locally cool these hotspots. Moreover, the efficiency of an hBN heat spreader in cooling such localized heated regions is currently unknown, mainly because local thermometry has not been used to assess the cooling efficiency of hBN heat spreaders. Finally, the hotspot dimensions for which hBN dissipates heat most effectively have not yet been established.

Here, we address these questions by demonstrating and quantifying the cooling of localized hotspots. The specific advantages of our approach are that (i) we use local thermometry to monitor the amount of heating of the localized hotspot itself; (ii) we use clean-transferred, high-thermal-conductivity, single-crystalline hBN heat spreaders; and (iii) we provide simulations that predict the effectiveness of hBN heat spreaders. Specifically, we employ the "hot pick-up" method[21] to transfer hBN flakes, which avoids polymer contamination at the interface. In addition, this approach

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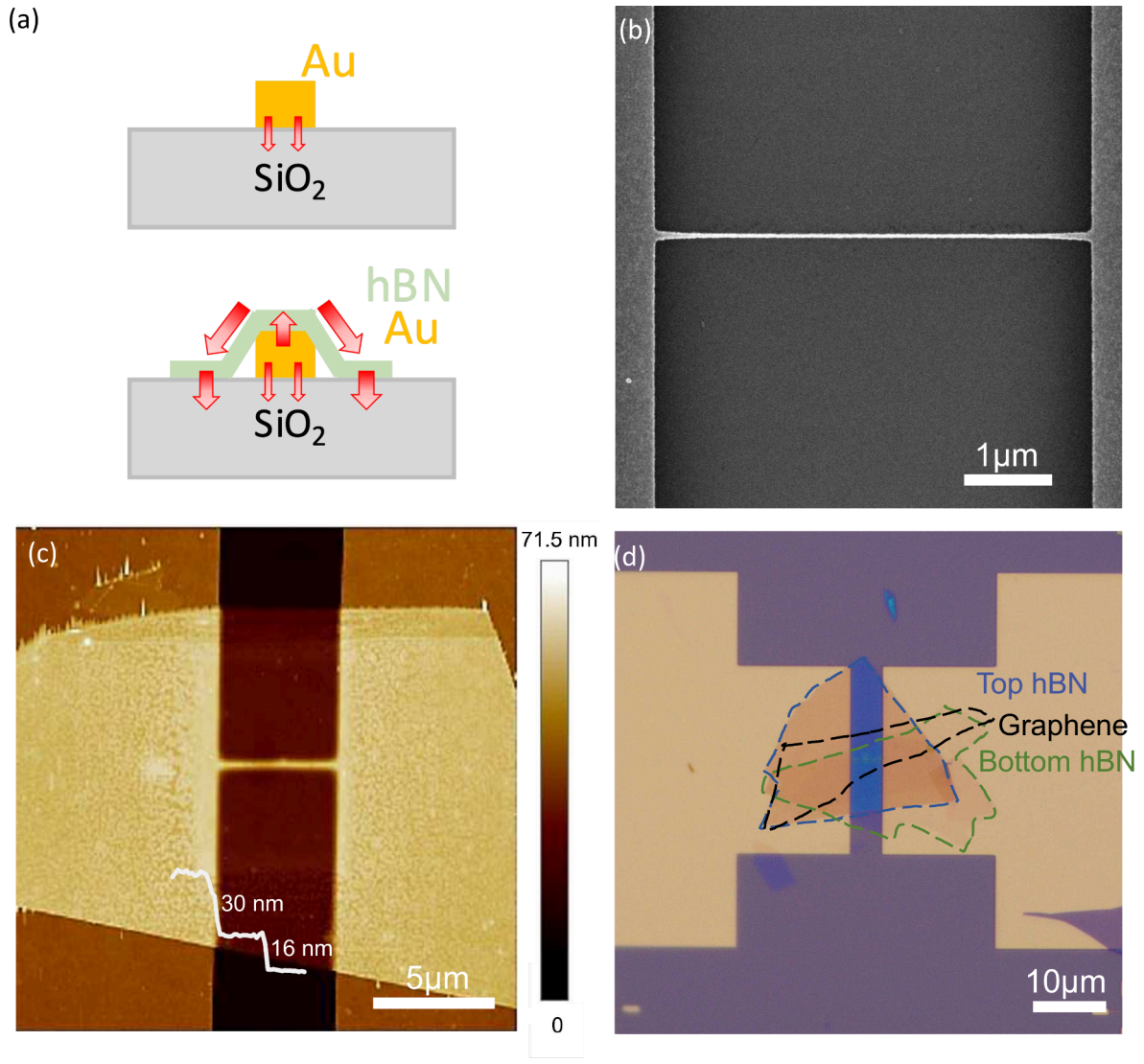

Figure 1. Images of representative samples for cooling electronic chip components. (a) Schematics of the improved cooling in the presence of an hBN flake. (b) Scanning Electron Microscopy (SEM) image of a gold nanostrip (E1 sample). (c) Atomic Force Microscopy (AFM) morphology of a gold nanostrip covered with hBN (E2 sample), showing no damage to the hBN flake after breakdown. Inset: height profile indicating steps due to hBN and the gold electrode. (d) Optical image of a gold nanostrip under an hBN/Gr/hBN stack (E3 sample), prepared for electrical measurements.

allows for the creation of heterostructures, including hBN-encapsulated graphene (Gr),[21,22] which preserves the high in-plane thermal conductivity of more than 1000 W m^{-1} K^{-1} of graphene,[23−25] while hydrodynamic effects can lead to short-lived thermal conductivities of more than 10,000 W m^{-1} K^{-1}.[26]

We will first show experiments demonstrating in-plane cooling of nanometer sized hotspots in electronic chip components, namely narrow gold nanostrips, using both hBN and hBN/Gr/hBN heat spreaders. Local thermometry is provided by the resistance change of the nanostrips with temperature. Next, we provide simulations showing that hBN is most efficient for cooling hotspots with lateral sizes below a few 100 nm. Subsequently, our attention will turn to the role of interfacial conductance. For this purpose, we investigate the cooling of relatively rough light-emitting hexagonal SiGe nanowires, as photonic chip components. We optically monitor the carrier temperature and show that a conformal hBN flake is able to increase the interfacial thermal conductance. Our results provide a clear route for efficient cooling of next-generation nanoscale chip components.

First, we used gold nanostrips as "model system" to assess the cooling capability of hBN flakes and hBN-based heterostructures, as shown schematically in Figure 1a. Such metal nanostrips are key components for interconnects in nanoelectronic devices.[27,28] The gold nanostrips (Figure 1b), with a length of 5 μm, a width of approximately 30 nm, as determined by Scanning Electron Microscopy (SEM), and a thickness of 30 nm, were patterned using electron beam lithography (EBL) followed by e-beam evaporation (see the Supporting Information (SI) for details). The hBN flakes and the hBN/Gr/hBN stacks were prepared by mechanical exfoliation followed by a "hot pick-up" technique[21] and subsequently transferred onto gold nanostrips (see SI). For fair comparison, only hBN flakes with a thickness of approximately 15 nm were selected, based on the color on the SiO_2/Si substrate[29] and Atomic Force Microscopy

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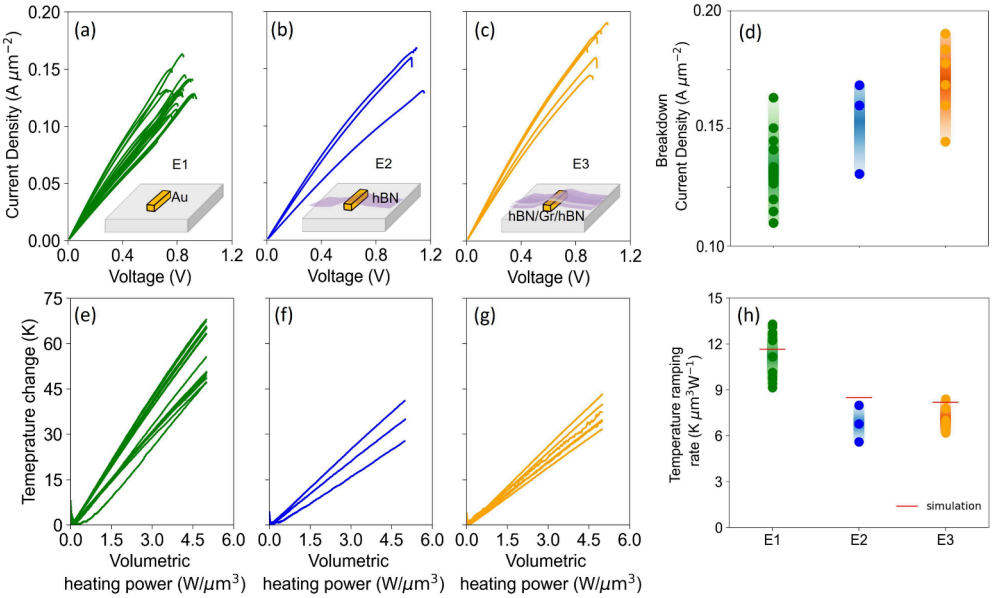

Figure 2. Assessing the cooling performance of hBN in electronic chip components through electrical measurements. (a)−(c) Current density of the Au nanostrips as a function of source-drain voltage for sample types E1 (a), E2 (b), and E3 (c). All samples break after reaching a certain input voltage. (d) Overview of the breakdown current densities of all measured samples of types E1, E2, and E3, showing increased breakdown current densities for sample types E2 and E3. (e)−(g) Temperature increase of Au nanostrips as a function of heating power density for sample types E1 (e), E2 (f), and E3 (g). (h) Overview of the temperature ramping rate of all measured samples of types E1, E2, and E3. The solid data points in panels (d) and (h) represent the measured values for individual samples, while the colored areas indicate the average and spread. Histograms of the data presented in panels (d) and (h) are provided in Figure S3. The solid red lines in (h) represent the results obtained using numerical simulations (see SI).

measurements, see Figure S11. This minimizes the influence of thickness-dependent out-of-plane thermal conductivities.[30]

We fabricated multiple samples of three categories: sample type E1, which are bare gold nanostrips (17 samples); sample type E2, which are gold nanostrips covered by hBN flakes (3 samples); and sample type E3, which are gold nanostrips covered by hBN/Gr/hBN stacks (6 samples). Figure 1 shows representative sample characterization of the three sample types. AFM topography measurements confirm good contact and no polymer residues at the interfaces between the hBN and the gold nanostrip (Figure 1c). The outline in Figure 1d shows the position of the hBN and graphene layers. We also employed Raman spectroscopy to characterize the encapsulated graphene, which is detailed in the SI (Figure S1).

To evaluate the heat dissipation performance of the hBN and hBN/Gr/hBN stacks, we recorded the electrical breakdown behavior induced by self-heating for the three sample types. We applied a voltage difference across the gold nanostrips and measured the resulting current (see SI). The current leads to Joule heating and eventually breakdown, as shown in Figures 2a−c. The breakdown current density is defined as the point where an abrupt drop to zero current occurs in the I−V characteristics, which is the result of the local melting of a small region of the Au nanostrip. The variation of the breakdown current within the same sample type arises from slight differences in surface roughness and sample width, which affect the heating behavior. Sample type E2 shows a higher average breakdown current density of 0.15 ± 0.02 A μm^{-2}, compared to sample type E1, which has an average breakdown current density of 0.13 ± 0.03 A μm^{-2}). For sample type E3, the average breakdown current density increased further to 0.17 ± 0.02 A μm^{-2} (Figure 2d), which is around 30% higher than sample type E1. This shows that covering gold nanostrips with hBN and hBN/Gr/hBN heterostructures leads to improved performance in terms of breakdown. We attribute this to improved heat dissipation around hotspots.

To confirm this, we monitored the temperature variation in the Au nanostrip, which provides an intrinsic characterization of thermal effects.[31] We used the temperature ramping rate of the nanostrip, which is the increase in temperature divided by heating power density, as a key indicator of the cooling efficiency provided by the nanostrip environment. We derived the temperature ramping rate of the nanostrips by using the resistance change of the nanostrips (see Figure S5) as a function of the heating power density. Figures 2e−g show the average increase in the temperature of the Au nanostrip as a function of the heating power density. As the heating power density increases, the temperature in sample type E1 increases strongly, corresponding to an average temperature ramping rate of 11.2 K μm^3 W^{-1} (Figure 2h). Instead, sample types E2 and E3 exhibit a lower average temperature ramping rate of 6.8 K μm^3 W^{-1}, which is around 40% lower than that of E1. These results indicate that both hBN and hBN/Gr/hBN provide efficient cooling of gold nanostrips. This is supported by our finding that hBN and hBN/Gr/hBN heat spreaders lead to a more uniform heat distribution across the nanostrip (see Figure S2). Finally we note that sample type E3 has a very similar temperature ramping rate as E2 in the (weak) linear heating regime, while the breakdown current density is improved for E3 compared to E2. We attribute this to improved heat dissipation in the strong heating regime near breakdown, where it is beneficial to have more material to dissipate heat.

Next, we validate the cooling performance of hBN, by performing numerical simulations using the same sample

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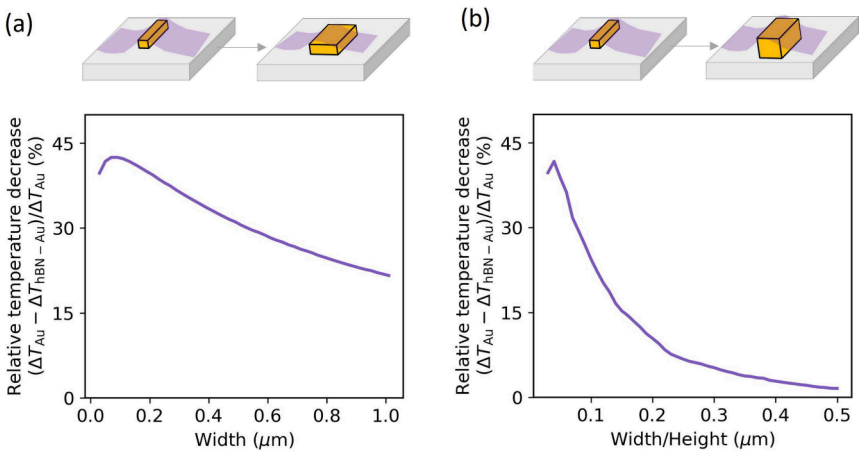

Figure 3. Numerical simulation of the cooling effect of hBN heat spreaders. (a) Relative temperature decrease of the Au nanostrip by the hBN heat spreader, as a function of the width of the nanostrip, where T_{Au} and T_{hBN-Au} are the temperature of the bare Au nanostrip (see Figure S4) and the temperature of the Au nanostrip with a hBN heat spreader, respectively. (b) Relative temperature decrease of a square cross-section Au nanostrip with an hBN heat spreader, as a function of width/height. The schematics in panels (a) and (b) illustrate how the geometry is being varied.

geometry as in the experiments (see SI, Figure S4). The Au nanostrips were modeled as uniform heaters with a power density of 5 mW μm^{-3}, while the bottom of the substrate was set as a heat sink. The thermal parameters of the materials, including the interfacial thermal conductance between materials, are provided in the SI. As shown in Figure S4, the heat generated in the Au nanostrip dissipates through the substrate for sample type E1; through hBN and the substrate for sample type E2; and through hBN/Gr/hBN and the substrate for sample type E3. We probed the average temperature change in the nanostrip and calculated the associated temperature ramping rate, which is the same observable as in the experiment. The simulation results are consistent with the experimental data, as shown as the red solid lines in Figure 2h, which confirms the effectiveness of the heat dissipation of one-dimensional heat sources by hBN.

Having established that hBN and hBN/Gr/hBN are effective in cooling gold nanostrips, we evaluate the size range in which hotspot cooling with an hBN heat spreader is most effective by simulating the cooling effect of hBN for structures with varying sizes (see Figure 3). For a structure with a fixed height of 30 nm, the most effective cooling occurs for a width of 80 nm (Figure 3a). When both width and height vary, the largest relative amount of cooling is observed at a width/height of 40 nm (Figure 3b). The results thus demonstrate that hBN is particularly suited for cooling localized heat in submicrometer-scale regions. It is less effective in cooling much larger components, as it is predominantly based on the spreading of heat in the in-plane direction.

Finally, we move to investigating the potential of hBN flakes as anisotropic heat spreaders for cooling a photonic building block, specifically hexagonal silicon−germanium nanowires. We chose these nanowires, because they feature very rough side facets on the nanoscale.[32] Therefore, they represent an exceptionally challenging case, due to the difficulties in achieving conformal coverage and reducing the thermal boundary conduction when using conventional heat spreaders. Furthermore, hexagonal SiGe alloys have recently emerged as promising and efficient direct bandgap light emitters for Si-based integrated photonics applications. This material exhibits a nanosecond optical lifetime, a tunable band gap from 0.35 to 0.67 eV for Ge-rich SiGe alloys with up to 35% silicon content, and is suitable for fabricating quantum wells with type I band alignment.[33−35] Its potential is further underscored by recent observations of stimulated emission in hexagonal SiGe nanowires, highlighting its suitability for silicon-compatible light sources.[36]

In our effort to assess the ability of hBN to dissipate heat in photonic building blocks, we grew hexagonal SiGe nanowires, as detailed in the SI. The nanowires were subsequently dispersed on a 400 nm thick aluminum nitride (AlN) layer, which has a relatively high thermal conductivity[36] of 165 W m^{-1} K^{-1}, grown on top of a sapphire (Al_2O_3) wafer. In spite of the high thermal conductivity of the AlN substrate, the primary limitation preventing these nanowires from achieving lasing remains the inadequate heat dissipation to the substrate under strong optical excitation. This is because nanowires have rough side surfaces as shown in Figure 4a,d, resulting in a very small effective contact area between the nanowire and the AlN/Al_2O_3 substrate, leading to a reduced thermal interface conductance. The resulting overheating rapidly decreases the optical gain at high excitation fluence.[36] Hexagonal SiGe nanowires thus provide a critical test case for the cooling performance of hBN flakes.

To prevent overheating at the nanoscale, we employed hexagonal boron nitride (hBN) flakes to dissipate the heat from the nanowire toward a gold heat sink deposited on top of the AlN/Al_2O_3 substrate. Due to the broadband optical absorption of graphene,[37] we only used hBN to cool the nanowires, discarding hBN/Gr/hBN heterostructures. We fabricated three sample types, using the same pick-up technique as for the nanostrips (see SI): sample type P1, which are nanowires transferred onto a bare AlN/Al_2O_3 substrate (as a reference); sample type P2, which is a nanowire on top of a 12 nm hBN flake, which in turn is positioned on an AlN/Al_2O_3 substrate; and sample type P3, which is a nanowire on an AlN/Al_2O_3 substrate, with the nanowire covered by a 12 nm hBN flake (schematic inset of Figure 4b). Additional sample types P4, which are nanowires on top of an "industry-standard" SiO_2/Si substrate without hBN, and sample type P5, which are nanowires on top of hBN flakes on a SiO_2/Si substrate, are discussed in Figures S7 and S9 of the Supporting Information.

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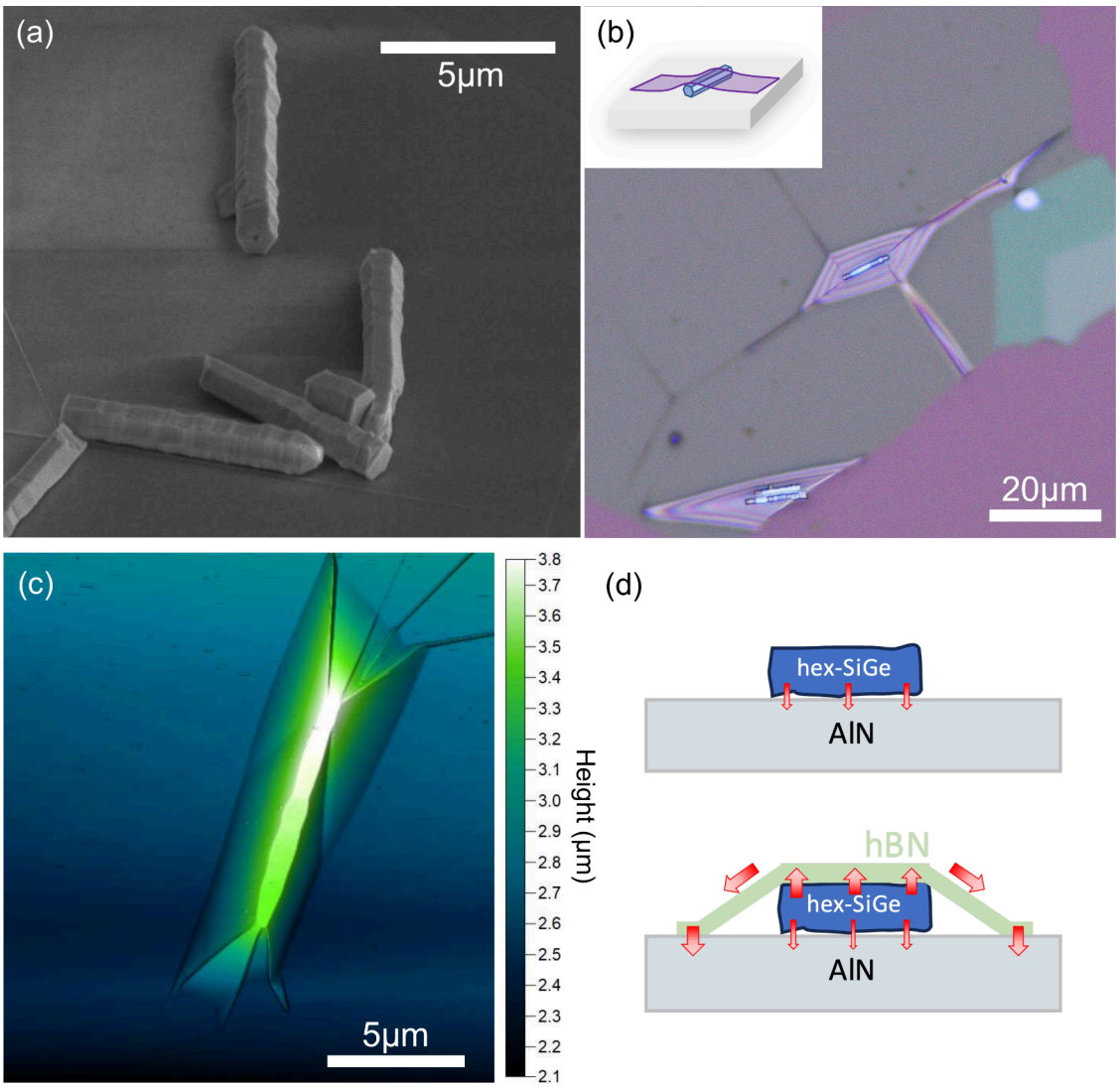

Figure 4. Images of representative samples for cooling optical chip components. (a) SEM image of hexagonal SiGe nanowires on an AlN/Al_2O_3 substrate.(b) Optical micrograph of a hexagonal $Si_{0.2}Ge_{0.8}$ nanowire covered by an hBN flake (gray) on an AlN/Al_2O_3 substrate (purple). The concentric interference pattern is caused by the hBN surface, descending between the nanowire top facet down to the substrate in a "tent-like" structure. (c) Representative Atomic Force Microscopy image of a nanowire under an hBN flake showing the conformal contact with the relatively rough nanowire top facet. (d) Schematics of the improved cooling in the presence of an hBN flake.

Figure 4c presents an AFM image of a representative P3 sample. The nanowire is conformally covered by the hBN flake, which adapts to its rough top facet, as visible in the center of the structure depicted in Figure 4c. The resulting "tent structure", formed by the hBN bending over the nanowire profile, is shown in the AFM image in Figure 4c, as well as in the optical microscope image in Figure 4b.

We first studied sample types P4 and P5, in which the hexagonal $Si_{0.2}Ge_{0.8}$ nanowires were heated by laser excitation and thus served as nanoscale diameter heaters on a commercially relevant SiO_2/Si substrate. For P4 nanowires, we observe that 8 out of 10 samples show a steep increase in detected blackbody radiation below an excitation level of 7.5 mJ cm^{-2} (see SI, Figure S7), hinting at catastrophic breakdown. By adding an hBN flake below the nanowires, we find that only 3 out of 8 nanowire samples showed this sudden increase in blackbody radiation below an excitation density of 7.5 mJ cm^{-2}, as shown in the SI. This suggests improved heat dissipation.

To obtain more quantitative information, we used the hexagonal $Si_{0.2}Ge_{0.8}$ nanowires simultaneously as heaters and as inherently calibrated local thermometers by deducing the carrier temperature from the high-energy Fermi−Dirac tail of the photoluminescence (PL) spectra. For this purpose, we characterized the emission properties of the nanowires using micro-PL spectroscopy (see SI). Figures 5a−c show the PL spectra of single nanowires in sample types P1, P2, and P3, as a function of the excitation power. All measurements were performed in a cryostat with a coldfinger temperature of 4 K using a femtosecond excitation laser with a wavelength of 1030 nm and a repetition rate of 40 MHz (see SI). To obtain the carrier temperature from these spectra, we used the Lasher−Stern−Würfel (LSW) approach. This is a generalization of Planck's law for a semiconductor under carrier injection, introducing a nonzero photon chemical potential equal to the quasi-Fermi level splitting and modulating the resulting emission by the absorption coefficient of the material.[34,38] Figure 5d shows the obtained carrier temperatures. Due to

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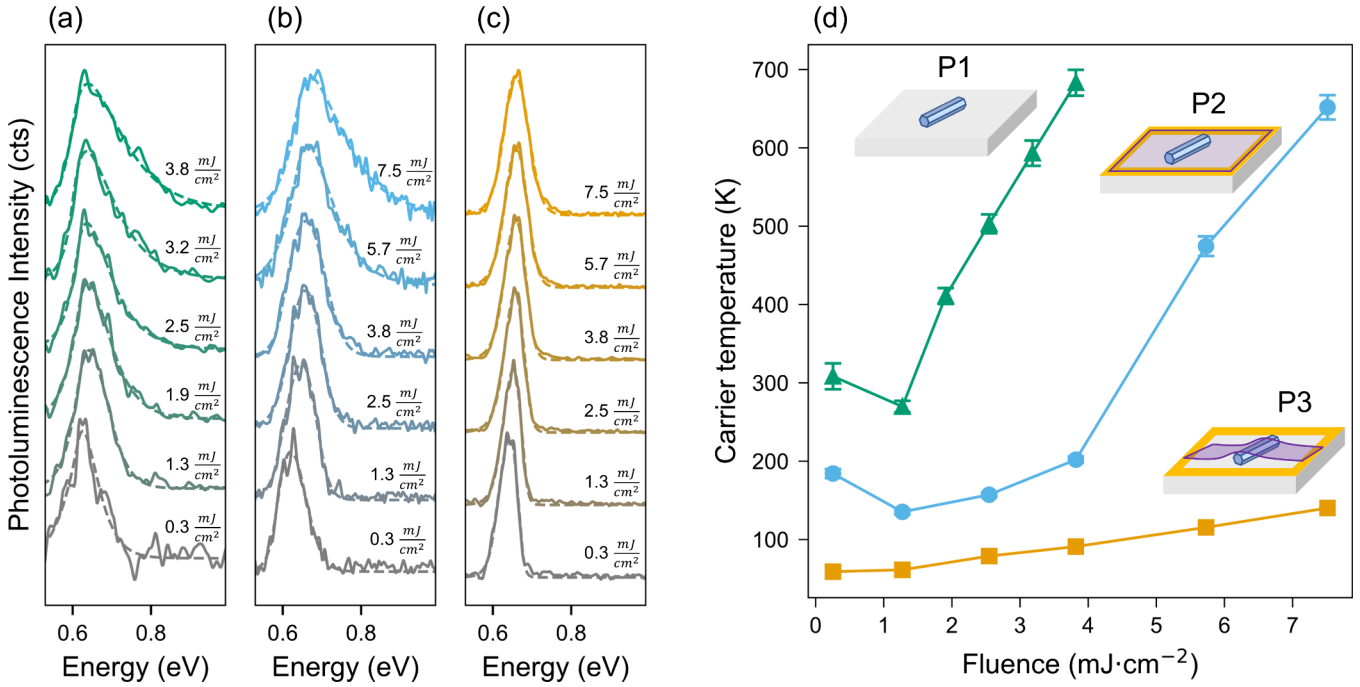

Figure 5. Assessing the cooling performance of hBN in photonic chip components through photoluminescence. (a–c) Time-averaged photoluminescence (PL) spectra as a function of excitation fluence for a single hexagonal $Si_{0.2}Ge_{0.8}$ nanowire in three sample configurations, as shown by the schematic insets in panel (d): (a) on the bare AlN/Al_2O_3 substrate (P1), (b) on top of a 12 nm-thick hBN flake, which is in turn deposited on a AlN/Al_2O_3 substrate (P2), and (c) on an AlN/Al_2O_3 substrate, and fully covered by the hBN flake (P3). The dashed lines show the LSW fits to each spectrum, which provide the carrier temperature. (d) Time-averaged carrier temperature as a function of excitation fluence at a cryostat temperature of 4K, for the three sample types: P1 (green triangles), P2 (blue circles), and P3 (yellow squares). When not visible, the error bars (68% confidence interval) are hidden by the marker.

efficient carrier cooling with a 180 ps relaxation time,[38] the carrier ensemble rapidly reaches quasi-equilibrium with the lattice after the short excitation pulse. In a first-order approximation (see Figure S8 for more details), this allows us to obtain the lattice temperature of the hexagonal $Si_{0.2}Ge_{0.8}$.

For sample type P1, the carrier temperature rapidly increases to 700 K at an excitation fluence of 4 mJ cm^{-2}, which we attribute to the poor interfacial thermal conductance between the nanowire and the substrate. The heat spreading capability of our hBN flakes becomes immediately apparent when we compare sample P2 with sample type P1. In sample P2, the increase in carrier temperature remains limited to 200 K at an excitation fluence of 4 mJ cm^{-2}, thus allowing measurements up to higher fluences. The enhanced thermal coupling for P2-like samples is further explored in Figure S7.

We observe even better cooling performance for sample P3, in which the carrier temperature remains limited below 150 K throughout the investigated fluence range (1–7.5 mJ cm^{-2}). As compared with P2, we explain the superior cooling in the P3 sample by the substantially increased interfacial thermal conductance G between the hBN heat spreader and the rough side walls of the hexagonal $Si_{0.2}Ge_{0.8}$ nanowire, as the hBN flake is capable of adapting and covering the nanoscale roughness of the side walls of the nanowire. The nanoscale adaption of the hBN flake to the rough interface of the nanowire is supposed to be absent in the P2 configuration, where the hBN flake covers and adapts to the flat substrate. A statistical analysis including a larger number of nanowires is presented in Figure S6.

The efficient cooling in sample P3 is explained by a two-step process (see Figure 4d) in which heat is first transferred from the nanowire to the hBN heat spreader. The efficiency of this first process is governed by the larger interfacial conductance between the rough nanowire and the highly conformal hBN flake. In the second step, the hBN heat spreader transfers the heat to the high-conductivity AlN substrate. In sample P1, however, the interfacial thermal conductance between the rough nanowire and the flat AlN substrate is much lower, resulting in a quick rise of the carrier temperature up to 700 K.

To quantitatively assess the enhanced heat dissipation in sample P3, we note that the temperature is about 6–7 times smaller than for sample P1, suggesting a 6–7 times increased interfacial thermal conductance. To verify that the temperature increase is inversely proportional to the interfacial thermal conductance, we performed COMSOL multiphysics simulations (see Figure S10). The simulation shows that the temperature increase in the hexagonal SiGe nanowire is indeed inversely proportional to the interfacial thermal conductance G between the nanowire and the AlN substrate (sample P1) or the hBN heat spreader (sample P3). To eliminate possible systematic errors due to cooling by blackbody radiation, we only consider the lowest measured fluence of 0.3 mJ cm^{-2} at which we observe a steady-state lattice temperature of 308, 184, and 58 K for samples P1, P2, and P3, respectively. Thus, we obtain a 2-fold and a 5-fold increase in interfacial thermal conductance for samples P2 and P3, respectively, with respect to sample P1.

In summary, by employing clean-transferred hBN flakes and hBN-based heterostructures, we effectively reduce the local temperature of electronic and photonic chip components due to improved in-plane heat dissipation and improved interfacial thermal conduction. These findings offer important insight

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into the intrinsic cooling properties of hBN flakes and provide guidance for the future design of devices with improved heat dissipation. Effective thermal management by hBN flakes enables higher working power densities in gold interconnects and offers a lower operating temperature of photonic devices, such as semiconductor lasers. We therefore envision an important role for hBN-based nanoscale thermal management in a broad range of electronic and photonic applications. For future work it would be interesting to perform direct measurements of the interfacial thermal conductance between hBN flakes and underlying materials or devices, to vary flake thickness(es), and to study alternative heat-spreading 2D materials, such as hexagonal AlN flakes.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.5c05376.

Additional methods and discussion, electrical experiments, and photonics experiments (PDF)

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Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Pop, E. Energy dissipation and transport in nanoscale devices. *Nano Research* **2010**, *3*, 147−169.

(2) Woon, W.-Y.; Kasperovich, A.; Wen, J.-R.; Hu, K. K.; Malakoutian, M.; Jhang, J.-H.; Vaziri, S.; Datye, I.; Shih, C. C.; Hsu, J. F.; Bao, X. Y.; Wu, Y.; Nomura, M.; Chowdhury, S.; Liao, S. S. Thermal management materials for 3D-stacked integrated circuits. *Nature Reviews Electrical Engineering* **2025**, *2*, 598−613.

(3) Chen, R.; Hochbaum, A. I.; Murphy, P.; Moore, J.; Yang, P.; Majumdar, A. Thermal Conductance of Thin Silicon Nanowires. *Phys. Rev. Lett.* **2008**, *101*, 105501.

(4) Hochbaum, A. I.; Chen, R.; Delgado, R. D.; Liang, W.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **2008**, *451*, 163−167.

(5) Franklin, A. D. Nanomaterials in transistors: From high-performance to thin-film applications. *Science* **2015**, *349*, aab2750.

(6) Waldrop, M. M. The chips are down for Moore's law. *Nature* **2016**, *530*, 144−147.

(7) Shahil, K. M. F.; Balandin, A. A. Graphene−Multilayer Graphene Nanocomposites as Highly Efficient Thermal Interface Materials. *Nano Lett.* **2012**, *12*, 861−867.

(8) Köroğlu, Ã.; Pop, E. High Thermal Conductivity Insulators for Thermal Management in 3D Integrated Circuits. *IEEE Electron Device Lett.* **2023**, *44*, 496−499.

(9) Yan, Z.; Liu, G.; Khan, J. M.; Balandin, A. A. Graphene quilts for thermal management of high-power GaN transistors. *Nat. Commun.* **2012**, *3*, 827.

(10) Bae, S.-H.; Shabani, R.; Lee, J.-B.; Baeck, S.-J.; Cho, H. J.; Ahn, J.-H. Graphene-Based Heat Spreader for Flexible Electronic Devices. *IEEE Trans. Electron Devices* **2014**, *61*, 4171−4175.

(11) Yan, Z.; Nika, D. L.; Balandin, A. A. Thermal properties of graphene and few-layer graphene: Applications in electronics. *IET Circuits, Devices & Systems* **2015**, *9*, 4−12.

(12) Akinwande, D.; et al. A Review on Mechanics and Mechanical Properties of 2D Materials−Graphene and Beyond. *Extreme Mechanics Letters* **2017**, *13*, 42−77.

(13) Song, H.; Liu, J.; Liu, B.; Wu, J.; Cheng, H.-M.; Kang, F. Two-Dimensional Materials for Thermal Management Applications. *Joule* **2018**, *2*, 442−463.

(14) Jiang, P.; Qian, X.; Yang, R.; Lindsay, L. Anisotropic thermal transport in bulk hexagonal boron nitride. *Physical Review Materials* **2018**, *2*, 064005.

(15) Kim, S. E.; Mujid, F.; Rai, A.; Eriksson, F.; Suh, J.; Poddar, P.; Ray, A.; Park, C.; Fransson, E.; Zhong, Y.; Muller, D. A.; Erhart, P.; Cahill, D. G.; Park, J. Extremely anisotropic van der Waals thermal conductors. *Nature* **2021**, *597*, 660−665.
(16) R, K.; Srivastava, A.; Midya, S.; Shanu, A.; Slathia, S.; Vandana, S.; Kar, S.; Glavin, N. R.; Roy, A. K.; Sreeram, P. R.; Singh, A. K.; Tiwary, C. S. Enhanced Heat Dissipation and Reduced Power Consumption in Electronics Using 2D Hexagonal Boron Nitride. *Small* **2025**, *21*, 2502007.
(17) Watanabe, K.; Taniguchi, T.; Kanda, H. Direct-bandgap properties and evidence for ultraviolet lasing of hexagonal boron nitride single crystal. *Nat. Mater.* **2004**, *3*, 404−409.
(18) Choi, I.; Lee, K.; Lee, C.; Lee, J. S.; Kim, S. M.; Jeong, K.; Kim, J. S. Application of Hexagonal Boron Nitride to a Heat-Transfer Medium of an InGaN/GaN Quantum-Well Green LED. *ACS Appl. Mater. Interfaces* **2019**, *11*, 18876−18884.
(19) Liu, D.; et al. Conformal hexagonal-boron nitride dielectric interface for tungsten diselenide devices with improved mobility and thermal dissipation. *Nat. Commun.* **2019**, *10*, 1188.
(20) Liu, D.; Chen, X.; Zhang, Y.; Wang, D.; Zhao, Y.; Peng, H.; Liu, Y.; Xu, X.; Wee, A. T. S.; Wei, D. Graphene Field-Effect Transistors on Hexagonal-Boron Nitride for Enhanced Interfacial Thermal Dissipation. *Advanced Electronic Materials* **2020**, *6*, 2000059.
(21) Purdie, D. G.; Pugno, N. M.; Taniguchi, T.; Watanabe, K.; Ferrari, A. C.; Lombardo, A. Cleaning interfaces in layered materials heterostructures. *Nat. Commun.* **2018**, *9*, 5387.
(22) Wang, L.; Meric, I.; Huang, P. Y.; Gao, Q.; Gao, Y.; Tran, H.; Taniguchi, T.; Watanabe, K.; Campos, L. M.; Muller, D. A.; Guo, J.; Kim, P.; Hone, J.; Shepard, K. L.; Dean, C. R. One-dimensional electrical contact to a two-dimensional material. *Science* **2013**, *342*, 614−617.
(23) Pak, A. J.; Hwang, G. S. Theoretical Analysis of Thermal Transport in Graphene Supported on Hexagonal Boron Nitride: The Importance of Strong Adhesion Due to -Bond Polarization. *Physical Review Applied* **2016**, *6*, 034015.
(24) Zhang, Z.; Hu, S.; Chen, J.; Li, B. Hexagonal boron nitride: a promising substrate for graphene with high heat dissipation. *Nanotechnology* **2017**, *28*, 225704.
(25) Karak, S.; Paul, S.; Negi, D.; Poojitha, B.; Srivastav, S. K.; Das, A.; Saha, S. Hexagonal Boron Nitride-'Graphene Heterostructures with Enhanced Interfacial Thermal Conductance for Thermal Management Applications. *ACS Applied Nano Materials* **2021**, *4*, 1951.
(26) Block, A.; Principi, A.; Hesp, N. C. H.; Cummings, A. W.; Liebel, M.; Watanabe, K.; Taniguchi, T.; Roche, S.; Koppens, F. H. L.; van Hulst, N. F.; Tielrooij, K.-J. Observation of giant and tunable thermal diffusivity of a Dirac fluid at room temperature. *Nat. Nanotechnol.* **2021**, *16*, 1195−1200.
(27) Trouwborst, M. L.; van der Molen, S. J.; van Wees, B. J. The role of Joule heating in the formation of nanogaps by electromigration. *J. Appl. Phys.* **2006**, *99*, 114316.
(28) Xiang, A.; Hou, S.; Liao, J. Tuning the Local Temperature during Feedback Controlled Electromigration in Gold Nanowires. *Appl. Phys. Lett.* **2014**, *104*, 223113.
(29) Anzai, Y.; Yamamoto, M.; Genchi, S.; Watanabe, K.; Taniguchi, T.; Ichikawa, S.; Fujiwara, Y.; Tanaka, H. Broad range thickness identification of hexagonal boron nitride by colors. *Applied Physics Express* **2019**, *12*, 055007.
(30) Jaffe, G. R.; Smith, K. J.; Watanabe, K.; Taniguchi, T.; Lagally, M. G.; Eriksson, M. A.; Brar, V. W. Thickness-Dependent Cross-Plane Thermal Conductivity Measurements of Exfoliated Hexagonal Boron Nitride. *ACS Appl. Mater. Interfaces* **2023**, *15*, 12545−12550.
(31) Bao, J.; Edwards, M.; Huang, S.; Zhang, Y.; Fu, Y.; Lu, X.; Yuan, Z.; Jeppson, K.; Liu, J. Synthesis and applications of two-dimensional hexagonal boron nitride in electronics manufacturing. *J. Phys. D: Appl. Phys.* **2016**, *49*, 265501.
(32) Vincent, L.; Fadaly, E. M.; Renard, C.; Peeters, W. H.; Vettori, M.; Panciera, F.; Bouchier, D.; Bakkers, E. P.; Verheijen, M. A. Growth-Related Formation Mechanism of I3-Type Basal Stacking Fault in Epitaxially Grown Hexagonal Ge-2H. *Advanced Materials Interfaces* **2022**, *9*, 2102340.
(33) Fadaly, E. M. T.; et al. Direct-bandgap emission from hexagonal Ge and SiGe alloys. *Nature* **2020**, *580*, 205−209.
(34) van Lange, V. T.; Dijkstra, A.; Fadaly, E. M. T.; Peeters, W. H. J.; van Tilburg, M. A. J.; Bakkers, E. P. A. M.; Bechstedt, F.; Finley, J. J.; Haverkort, J. E. M. Nanosecond Carrier Lifetime of Hexagonal Ge. *ACS Photonics* **2024**, *11*, 4258−4267.
(35) Peeters, W. H. J.; van Lange, V. T.; Belabbes, A.; van Hemert, M. C.; Jansen, M. M.; Farina, R.; van Tilburg, M. A. J.; Verheijen, M. A.; Botti, S.; Bechstedt, F.; Haverkort, J. E. M.; Bakkers, E. P. A. M. Direct bandgap quantum wells in hexagonal Silicon Germanium. *Nat. Commun.* **2024**, *15*, 5252.
(36) van Tilburg, M. A. J.; Farina, R.; van Lange, V. T.; Peeters, W. H. J.; Meder, S.; Jansen, M. M.; Verheijen, M. A.; Vettori, M.; Finley, J. J.; Bakkers, E. P. A. M.; Haverkort, J. E. M. Stimulated emission from hexagonal silicon-germanium nanowires. *Communications Physics* **2024**, *7*, 328.
(37) Nair, R. R.; Blake, P.; Grigorenko, A. N.; Novoselov, K. S.; Booth, T. J.; Stauber, T.; Peres, N. M. R.; Geim, A. K. Fine structure constant defines visual transparency of graphene. *Science* **2008**, *320*, 1308.
(38) Schouten, M. F.; van Tilburg, M. A. J.; van Lange, V. T.; Peeters, W. H. J.; Farina, R.; Jansen, M. M.; Vettori, M.; Bakkers, E. P. A. M.; Haverkort, J. E. M. Carrier cooling in direct bandgap hexagonal silicon-germanium nanowires. *Appl. Phys. Lett.* **2024**, *125*, 112106.

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